Low Power Transceiver ASIC Development

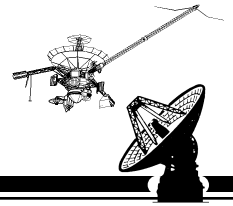
UPN 315-90-16

David Zillig

Semi-Annual Review of the FY97 SOMO/MO&DSD Technology Development Program

April 15, 1997

Low Power Transceiver ASIC Development
Objective and Significance



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Overall Objective

Develop and design an ASIC or FPGA chip set which will enable the design and future implementation of a low power TDRSS compatible transceiver. This transceiver would use the ASIC/FPGA along with the new low power CCD, the ATC-LP, to reduce size and power consumption.

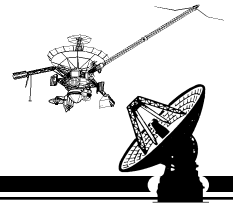
Goals

- **ASIC/FPGA Design: Develop an ASIC or FPGA design which performs the major acquisition and tracking functions for a TDRSS compatible DG1 Mode 2 BPSK signal for data rates up to 150 KBPS with rate 1/2 convolutional encoding.**

Significance

- **Such a chip or chip set in conjunction with the new low power CCD will be the enabling technology for the next generation TDRSS low power transceiver architecture.**

Low Power Transceiver ASIC Development
Objective and Significance (Cont'd)



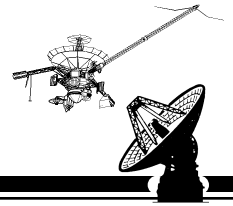
Goals

- **FPGA Evaluation Board Design: Produce a circuit board design which can fully exercise the FPGA designed. The card should allow isolated part testing as well as actual transceiver functionality. The board will include the CCD front end, a control processor and all required data handling circuitry for the potential of full system operation.**
- **ASIC Design Evolution: Have the first version of the full ASIC designed, simulated and ready for fabrication.**

Significance

- **The evaluation board will be an invaluable tool for verifying the FPGA design. Though the chip will be fully simulated, there is no substitute for actual hardware testing. This platform will allow such testing both at the chip and operational system level. It will be designed to interface with existing transceiver hardware whenever possible.**
- **Once all the basic algorithms have been verified using the FPGA evalustion board, the next step will be to move toward a full ASIC design.**

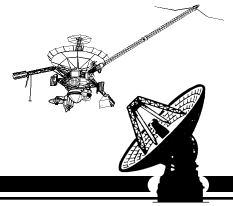
Low Power Transceiver ASIC Development
FY97 Accomplishments (Cont'd)



FPGA Evaluation Board Design

- **Defined basic evaluation board requirements which include isolated FPGA testing as well as transceiver functional performance.**
- **Developed evaluation board block diagram.**
- **Completed detailed circuit design for evaluation board:**
- **Fabrication of FPGA evaluation board nearing completion.**

Low Power Transceiver ASIC Development
FY97 Goals



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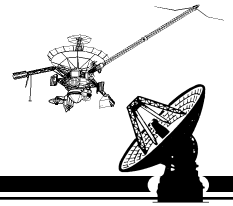
- **<u>FPGA Evaluation Board Fabrication, Integration and Test</u>: The evaluation board would be laid out, fabricated, debugged and tested. The FPGA chip would be evaluated and tested using this circuit card.**
- **<u>FPGA to ASIC Design Evolution</u>: Once all basic algorithms have been verified using the FPGA evaluation board, the next step would be to move toward a full ASIC design which would incorporate additional major transceiver functions. These could include the high speed NCOs, Viterbi decoder, microcontroller and clocking circuitry. Test plans and chip test vectors must be generated. Chip vendors would be contacted and consulted for risk reduction.**
- **<u>ASIC Ready for Fabrication</u>: Have the first version of the full ASIC designed, simulated and ready for fabrication.**

Low Power Transceiver ASIC Development Schedule



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Task	FY96				FY97				FY98		FY99	FY00	FY01	FY02
	Q1	Q2	Q3	Q4	Q1	Q2	Q3	Q4	Q1/2	Q3/4				
•FPGA Evaluation Board Fab/I&T(Goal #1)														
•FPGA to ASIC Design Evolution (Goal #2)														
•ASIC Ready for Fabrication (Goal #3)														